

**Amendments to the Claims:**

1. (Previously Presented) A semiconductor package comprising:

a plurality of horizontal metal leads, each of the leads having a first side, an opposite second side, and an inner end, wherein the inner ends of the leads each face a central region in a horizontal plane of the leads;

a first semiconductor chip having input/output pads, said first chip located in the central region;

a second semiconductor chip having central input/output pads and peripheral input/output pads, wherein each of the central input/output pads superimposes and is electrically connected to a respective one of the input/output pads of the first semiconductor chip, and each of the peripheral input/output pads superimposes and is electrically connected to the first side of a respective one of the leads; and

a package body formed of a hardened encapsulating material, wherein at least portions of the first and second semiconductor chips are encapsulated in the package body, and at least a portion of the second side of each of the leads is exposed at a horizontal first exterior surface of the package body.

2. (Previously Presented) The semiconductor package of claim 1, wherein the second side of each of the leads includes at least one recessed horizontal surface covered by said encapsulating material.

3. (Previously Presented) The semiconductor package of claim 1, wherein the second side of each of the leads includes a recessed horizontal surface at the inner end of the lead, said recessed horizontal surface being covered by said encapsulating material.

4. (Original) The semiconductor package of claim 1, wherein the second sides of the leads exposed at said first exterior surface collectively form rows and columns.

5. (Withdrawn)

6. (Withdrawn)

7. (Withdrawn)

8. (Previously Presented) The semiconductor package of claim 1, wherein the input/output pads of the first semiconductor chip are each electrically connected to the central input/output pads of the second semiconductor chip, and the peripheral input/output pads of the second semiconductor chip are each electrically connected to respective ones of the first sides of the leads, by one of a reflowed metal ball and an anisotropic conductive film.

9. (Withdrawn)

10. (Withdrawn)

11. (Previously Presented) The semiconductor package of claim 1, further comprising an insulative layer on the first side of each of the leads, wherein the peripheral input/output pads of the second semiconductor chip are electrically connected to the first sides of respective ones of the leads through said insulative layer.

12. (Withdrawn)

13. (Withdrawn)

14. (Withdrawn)

15. (Withdrawn)

16. (Withdrawn)

17. (Withdrawn)

18. (Withdrawn)

19. (Withdrawn)

20. (Withdrawn)

21. (Withdrawn)

22. (Withdrawn)

23. (Withdrawn)

24. (Withdrawn)

25. (Withdrawn)

26. (Withdrawn)

27. (Withdrawn)

28. (Previously Presented) A semiconductor package comprising:

a plurality of horizontal metal leads, each of the leads having a first side, an opposite second side, and an inner end wherein the second side of each of the leads includes at least one recessed horizontal surface and the inner ends of the leads face a central chip placement region;

first and second semiconductor chips stacked in said chip placement region, each of said chips having input/output pads, wherein at least some of the input/output pads of the first semiconductor chip face and are electrically connected to respective ones of the input/output pads of the second semiconductor chip by a first conductor, and other input/output pads of one of the first and second semiconductor chips are over the first sides of the leads and are each electrically connected to the first side of a respective one of the leads by a second conductor; and

a package body formed of a hardened encapsulating material, wherein at least portions of the first and second semiconductor chips and the conductors are encapsulated in the package body, the recessed horizontal surface of each of the leads is covered by the encapsulating material, and at least a portion of the second side of each of the leads is exposed at a horizontal first exterior surface of the package body.

29. (Withdrawn)

30. (Previously Presented) The semiconductor package of claim 28, wherein the input/output pads over the first sides of the leads each face and are electrically connected to respective ones of the first sides of the leads.

31. (Previously Presented) The semiconductor package of claim 28, wherein the first and second conductors are each a reflowed metal ball.

32. (Previously Presented) The semiconductor package of claim 28, wherein the first and second conductors are each an anisotropic conductive film.

33. (Original) The semiconductor package of claim 28, wherein one of the first and second semiconductor chips is in a horizontal plane with the leads in said chip placement region.

34. (Previously Presented) The semiconductor package of claim 28, further comprising an insulative layer on the first side of each of the leads, wherein certain ones of

the input/output pads of the second semiconductor chip are electrically connected to the first sides of respective ones of the leads through the insulative layer.

35. (Previously Presented) The semiconductor package of claim 28, wherein the second sides of the leads exposed at the first exterior surface collectively form rows and columns.

36. (Previously Presented) The semiconductor package of claim 1, wherein the peripheral input/output pads of the second semiconductor chip superimposing the first sides of the leads each face and are electrically connected to respective ones of the first sides of the leads.

37. (Previously Presented) The semiconductor package of claim 1, wherein the first semiconductor chip is in a horizontal plane with the leads in the central region.

38. (Currently Amended) A semiconductor package comprising:

a plurality of leads each defining opposed first and second sides and an inner end, the leads being arranged such that the inner ends collectively define a central region;

a first semiconductor chip disposed in the central region and having a plurality of input/output pads;

a second semiconductor chip having a plurality of central input/output pads and a plurality of peripheral input/output pads, each of the central input/output pads ~~superimposing and~~ being **aligned with and** electrically connected to a respective one of the input/output pads of the first semiconductor chip, with each of the peripheral input/output pads ~~superimposing and~~ being **aligned with and** electrically connected to the first side of a respective one of the leads; and

a package body at least partially encapsulating the leads and the first and second semiconductor chips such that at least a portion of the second side of each of the leads is exposed in an exterior surface of the package body.

39. (Previously Presented) The semiconductor package of claim 38, wherein the second side of each of the leads includes at least one recessed surface which is covered by the package body.

40. (Previously Presented) The semiconductor package of claim 38, wherein the second side of each of the leads includes a recessed surface which extends to the inner end and is covered by the package body.

41. (Previously Presented) The semiconductor package of claim 38, wherein the second sides of the leads exposed in the package body collectively form rows and columns.

42. (Previously Presented) The semiconductor package of claim 38, wherein the input/output pads of the first semiconductor chip are electrically connected to respective ones of the central input/output pads of the second semiconductor chip, and the peripheral input/output pads of the second semiconductor chip are electrically connected to respective ones of the first sides of the leads by a reflowed metal ball.

43. (Previously Presented) The semiconductor package of claim 38, wherein the input/output pads of the first semiconductor chip are electrically connected to respective ones of the central input/output pads of the second semiconductor chip, and the peripheral input/output pads of the second semiconductor chip are electrically connected to respective ones of the first sides of the leads by an anisotropic conductive film.

44. (Previously Presented) The semiconductor package of claim 38, further comprising an insulative layer disposed on the first side of each of the leads, the peripheral input/output pads of the second semiconductor chip being electrically connected to the first sides of respective ones of the leads through the insulative layer.

45. (Previously Presented) The semiconductor package of claim 38, wherein the peripheral input/output pads of the second semiconductor die each face and are electrically connected to respective ones of the first sides of the leads.

46. (Previously Presented) The semiconductor package of claim 38, wherein the first semiconductor chip defines a surface which extends in generally co-planar relation to the first surfaces of the leads.